EVENING

20 JAN 2023

[Total No. of Questions: 09]
Uni. Roll No. .....

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Program: B.Tech. (Batch 2018)
Semester: 4th
Name of Subject: Computer Architecture and Microprocessor
Subject Code: PCIT-108
Paper ID: 16237

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1. Parts A and B are compulsory
2. Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3. Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a. Compare operation code and operand with suitable example.
b. Determine the number of clock cycles that it takes to process 300 tasks in a 6-segment pipeline.
c. Differentiate software and hardware interrupt.
d. Elaborate MOV and MVI instructions with suitable example of both.
e. Define Embedded Systems.
f. What do you mean by Cache Coherence?

Part B **[Marks: 04 each]**

Q2. Compare 1-byte, 2-byte and 3-byte instructions.

Q3. Write an assembly language program to swap two numbers.

Q4. Differentiate Hardwired and Microprogrammed Control Unit

Q5. Elaborate the different phases of Instruction Cycle.

Q6. Explain Auxiliary Memory and its devices.

Q7. Discuss the various Memory Reference Instructions.

P.T.O.

Part – C

[Marks: 12 each]

Q8. Explain how RISC and CISC architectures differ. Describe some major characteristics of RISC architecture.

OR

What is micro controller? Discuss the architecture of 8051 microcontroller.

Q9. Explain various Addressing modes with suitable example of each.

OR

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-

1. Pipeline cycle time
2. Non-pipeline execution time
3. Speed up ratio
4. Pipeline time for 1000 tasks
5. Sequential time for 1000 tasks
6. Throughput

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