Please check that this question paper contains 09 questions and 02 printed pages within first ten minutes.

[Total No. of Questions: **09**] [Total No. of Pages: **02**]

Uni. Roll No. .....

B.Tech. (2018 Batch onwards)
Semester: 4th
DIGITAL ELECTRONICS
Subject Code: **PCEE-105**
Paper ID: **16186**

Time Allowed: 03 Hours **Max. Marks: 60**

Note:

1) **Part A and B are compulsory**
2) **Part-C** has two questions Q8 & Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately.
4) Here ' **sign** means complement.

Part – A **[Marks: 02 each]**

Q1.

a) Do the following conversions:
   i) (1101101.1011) to ( )10
   ii) (10110010) to ( )2's complement

b) Draw an EX-NOR gate. Write its Boolean expression and truth table.

c) Which Flip-Flop is normally not used in practical applications? Give reason for that.

d) State any two differences between RAM and ROM.

e) A 4 bit flash ADC is used for converting analog signal to digital signal. Calculate the number of comparators to be used in the circuit.

f) What is the range of voltage for CMOS for LOW and HIGH logic for +5V system?

Part – B **[Marks: 04 each]**

Q2. State and prove De-Morgans theorem with the help of truth table and logic diagrams.
Q3. Implement NOT, AND, OR and NAND gates using NOR gate(s) only.
Q4. Explain with logic circuit diagram and truth table the working of clock triggered JK Flip-Flop.

Q5. Design a Decimal to BCD Encoder.
Q6. Show how a PAL is programmed for a following 3-variable logic function

$$X=A'B'C + A'BC' + AC + AB'$$

Q7. What does the following circuit represent? Explain the operation of this circuit. What

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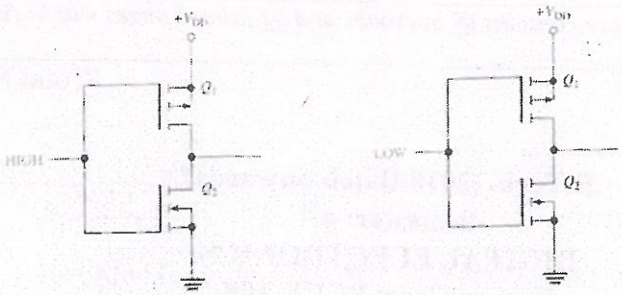
will be the conditions of Q1 and Q2 in both cases? Fig1(LHS).



Part – C **[Marks: 12 each]**

Q8. Use a Karnaugh map to minimize the following SOP expression:
X= B'C'D' + ABC'D'+ A'BC'D'+ A'B'CD+ AB'CD+ A'BCD'+ A'B'CD'+ ABCD'+ AB'CD'
Implement the simplified expression using logic gates

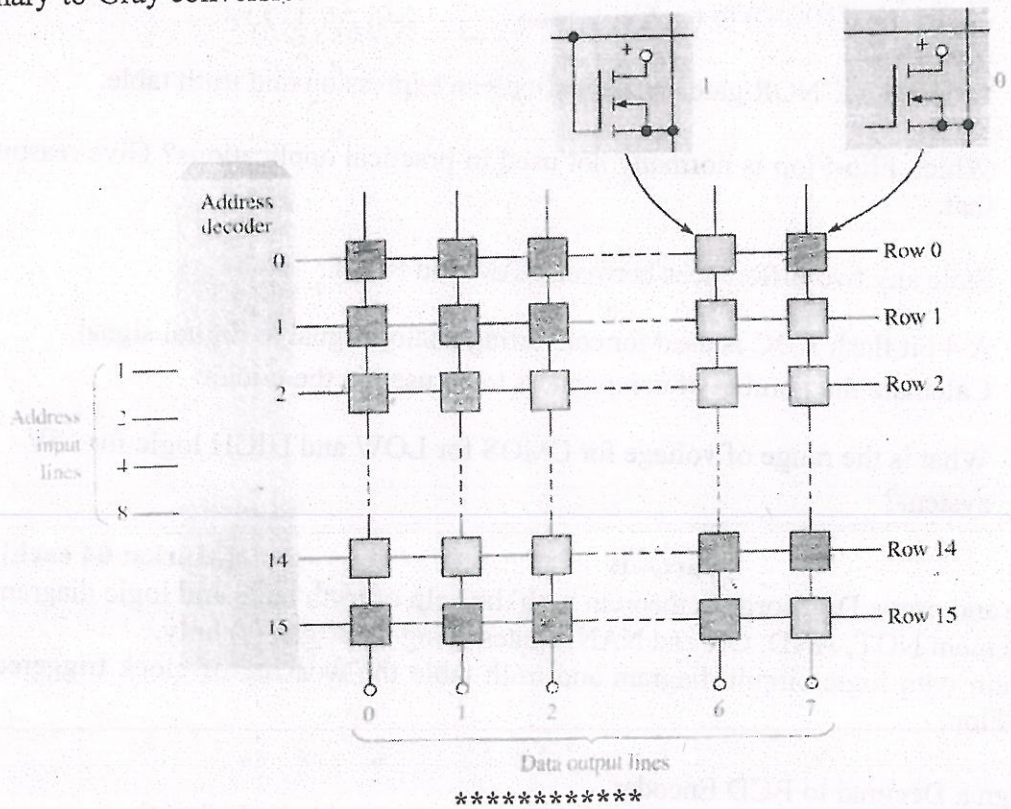
OR

Explain with block diagram the working of Dual Slope Analog-to-Digital converter.

Q9. Design a 3-bit Gray code synchronous counter and implement the counter using JK Flip-Flops.

OR

Show a basic ROM similar to one shown in figure below programmed for a 4-bit binary-to-Gray conversion.



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