Please check that this question paper contains 9 questions and 1 printed page within first ten minutes.

[Total No. of Questions: 09] [Total No. of Pages: 02]

Uni. Roll No. …….

Program: B.Tech
Semester: 3rd
Name of Subject: Computer Architecture
Subject Code: PCEC-105
Paper ID: 16035

Time Allowed: 02 Hours **Max. Marks: 60**

21-01-2022(M)

NOTE:

1) Each question is of 10 marks.
2) Attempt any six questions out of nine.
3) Any missing data may be assumed appropriately.

Q1. Explain various mechanisms of data transfer from any peripheral device.

Q2. Elaborate various types of addressing modes with the help of suitable examples.

Q3. Discuss in detail the organization of CPU in a digital computer. Also, differentiate between the terms "instruction interpretation" and "instruction sequencing".

Q4. Explain in detail the mappings used for Cache memory.

Q5. Elaborate on "Flynn's classification of computers". With proper reasoning, explain which architecture is of theoretical interest only and no practical system has been developed on it.

Q6. Compare and contrast the detailed architecture of RISC and CISC.

Q7. With suitable examples, explain Vector Computation.

Q8. Consider the following memory values and a one-address machine with an accumulator, What values do the following instructions load into accumulator?

Word 20 contains 40

Word 30 contains 50

Word 40 contains 60

Word 50 contains 70

Instructions are-

Load immediate 20

Load direct 20

Load indirect 20

Load immediate 30

Load direct 30

Load indirect 30

Q9. Consider three processes, all arriving at time zero, with total execution time of 10, 20 and 30 units respectively. Each process spends the first 20% of execution time doing I/O, the next 70% of time doing computation, and the last 10% of time doing I/O again. The operating system uses a shortest remaining compute time first scheduling algorithm and schedules a new process either when the running process gets blocked on I/O or when the running process finishes its compute burst. Assume that all I/O operations can be overlapped as much as possible. For what percentage of does the CPU remain idle?

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