Please check that this question paper contains_____ questions and _____ printed pages within first ten minutes.

[Total No. of Questions: 09] [Total No. of Pages: .....]

Uni. Roll No. …….

Program: B.Tech
Semester: 3rd
Name of Subject: Digital Electronics
Subject Code: PCEC-104
Paper ID: 16034

19-01-2022(M)

Time Allowed: 02 Hours **Max. Marks: 60**

NOTE:

1) Each question is of 10 marks.
2) Attempt any six questions out of nine
3) Any missing data may be assumed appropriately

Q1. Design a counter with the repeated binary sequence: 0, 1, 2, 3, 4, 5, 6 using J-K flip flop by avoiding lock out condition.

Q2. Solve using Q-M method and verify the result with K-map. Also implement using NOR gates only. $F(v,w,x,y,z)= \Sigma m (0,1,2,4,5 ,14,15,19,23,25,27,29,31)+d(7,8,9,11)$

Q3. How much computer memory (in bytes) would be required to store 10 seconds of a sensor signal sampled by a 12-bit A/D converter operating at a sampling rate of 5kHz?

Q4. A process is defined by the logical expression,

$$Z = AB + B\overline{C} + CD + B\overline{D} + BC$$

Reduce the above expression to minimum no. of literals using:

a. Boolean algebra
b. K-map

Q5. Design MOD-6 up-down counter using D flip-flops.

Q6. Give the comparison of TTL, ECL and CMOS basis on various parameters (give the approximate numerical values).

Q7. (a) If x=1101.101 and y= 100.1011, evaluate

I. x+y
II. x-y (using 1's complement)
III. y-x (using 2's complement)

(b) Mention the applications of ASCII, Excess-3 and Gray codes.

Q8. (a) Explain in detail how the invalid state of RS flip flop is removed in JK flip flop. Define toggle state in JK flip flop.

(b) Design a T flip flop by using JK flip flop. Also write its applications.

Q9.(a) Design a SIPO shift register. Also draw the timing diagram for the same.
(b) Explain Successive Approximation (SAR) ADC.

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