Please check that this question paper contains 9 questions and 2 printed pages within first ten minutes.

MORNING

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Uni. Roll No. .....

Program: B.Tech. (Batch 2018 onward)
Semester: 3rd
Name of Subject: **Digital Electronics**
Subject Code: **ESCS-101**
Paper ID: 16012

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a) How do Demultiplexer differ from Decoder?

b) Why do we need shift registers ?

c) An 4 bit D/A converter has an output range of '0' to'1.5V'. Calculate its resolution.

d) Evaluate $(110110)_2 - (10110)_2$ using 2's complement.

e) Evaluate (1001011)2 ÷ (11)2 using the long-division method.

f) Convert the BCD code number 000101000 1110101 into equivalent decimal value.

Part – B **[Marks: 04 each]**

Q2. Differentiate between static MOS and Dynamic MOS RAM. Explain the working of a static RAM cell with the help of a circuit diagram.

Q3. Draw and explain the working of 4-bit parallel adder circuit using full adders..

Q4. Convert D Flip-Flop to SR Flip –Flop.

Q5. Explain in detail the architecture of a programmable logic device.

Q6. Implement the following Boolean expression using NAND gates only.

$Y = A + \bar{B}C + AC$

Q7. Reduce the following expression using Boolean algebra

$$\left[A\left(B + \bar{C}\left(\overline{AB + A\bar{C}}\right)\right)\right]$$

Part – C **[Marks: 12 each]**

Q8. Design mod-8 synchronous counter using T flip-flops.

OR

a) Draw the circuit of R-2R ladder D/A converter and explain its operation.

b) Design parallel-In-Serial shift register. Explian in detail.

Q9. Design a 4-bit Binary to Gray Code converter.

OR

Design a digital system whose output is defined as logically low if the 4-bit input binary number is a multiple of 3; otherwise, the output will be logically high. The output is defined if and only if the input binary number is greater than 2. Design system by obtaining the simplified expressions in POS and SOP form.

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