Please check that this question paper contains____09__ questions and _2____ printed pages within first ten

[Total No. of Questions: 09] [Total No. of Pages: .....]

Uni. Roll No. .....

MORNING

27 DEC 2022

Program: B.Tech. (Batch 2018 onward)

Semester: 3rd

Name of Subject: Digital Circuits and Logic Design

Subject Code: ESIT-101

Paper ID: 16042

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a) Define 1's complement and 2's complement.

b) What are the various uses of VHDL?

c) Illustrate the advantages of Ring Counter.

d) Write a short note on SOP and POS.

e) Convert $(10101)_2$ to decimal.

f) Compare encoder and decoder.

Part – B **[Marks: 04 each]**

Q2. State and prove De-Morgan's Theorem.

Q3. What are universal gates? Realize the following gates using universal gates:

a. AND b. EX-NOR

Q4. Illustrate the working of Master Slave J-K flip flop.

Q5. Reduce the following Boolean expression: x'y'z +yz+ xz.

Q6. What is full subtractor? Draw a full subtractor circuit.

Q7. Explain the working of Gray code. Write its importance and its uses.

Part – C **[Marks: 12 each]**

Q8. Write short note on following:

a. RTL logic family **(6 marks)**

b. R-2R Ladder **(6 marks)**

OR

Design an 8 ×1 multiplexer using 4×1 and 2×1 multiplexer.

Q9. Design 2-bit Synchronous Up counter using JK flip flop.

OR

Minimize the following Boolean function-

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$$

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